A New Approach to High-Speed High-Resolution Capacitive Ratio Measurement

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Abstract - **This paper presents a new measurement method that is able to obtain high resolution within limited measurement range, without relying on time consuming oversampling technique. The theory behind is explained and are supported by simulation results.**

Keywords – **Capacitive ratio measurement, high speed, high resolution**

I. Introduction

In many applications involving capacitive sensors, the precise measurement of a capacitance ratio in a digital form is very important. When measurement resolution approaches the range of several ppm, switched-capacitor sigma-delta converter technique is often employed due to its robustness and its ability to achieve high measurement resolution [1]. In [1], measurement resolution down to 2 ppm had been reported.

Sigma-delta technique is an over-sampling technique. To reach a high measurement resolution, a large oversampling ratio needs to be employed. Therefore, this technique basically trades off resolution with measurement speed. In a commercial product based on this principle [2], the conversion time is in the order of hundreds of milli-seconds when resolution of 20 bit is needed. While this is perfectly fine for most of the applications where measurement speed is not an issue, in some applications, conversion time needs to be less than tens of micro seconds, and the resolution requirement still approaches 20 bit. Theoretically, the conversion time of sigma-delta converters can be increased by increasing the clock frequency. Such a solution unfortunately also increases the power consumption of the circuit. On the other hand, the clock frequency of a sigma-delta converter cannot be increased infinitely due to constraints in the required on-resistance of the MOS switches and other circuit non-idealities, such as charge injection. It is highly desirable to find a technique that can achieve high resolution measurement while still can retain relatively low power consumption.

Analog circuit design is about making compromises. Since measurement time cannot be sacrificed, something else needs to give its priority to other more important specifications. This paper deals with a measurement technique that trades off resolution with measurement range. In other words, high resolution is only attained within a limited measurement range. Outside this range, the resolution will deteriorate. As will be made clear in the following section, typical capacitive sensors show capacitance variation much smaller than their nominal values. Hence this trade-off is normally acceptable.

This paper is organized in 5 sections. Section II explains why usually measurement range of capacitive ratio is small. Section III presents the theoretical background for the proposed capacitive ratio measurement method. The simulation results for the proposed method will be given in section IV. The paper ends with some conclusions in section V.

II. Typical Capacitive Sensors

Capacitive sensors have wide range of applications, including position, acceleration, and humidity measurement. The discussions in this paper focus on capacitive position sensors, although the obtained conclusion can also be applied to other types of capacitive measurements. Parallel plate capacitive sensors are the most commonly utilized structure in position measurement. The two plates (or electrodes) of the sensor have to be mounted on the two objects whose relative position is of interest. Ideally, the initial stand-off distance between two plates of the capacitive sensor should be made as close as possible to the maximum expected relative movement between the two objects, to optimally make use of the dynamic range of the readout electronics.

In some situations, where the variation in the position of basically static objects needs to be accurately measured, the maximum expected relative movement is in the order of several tens of nanometers. Placing capacitive sensor electrodes distance to such distances is very impractical due to mounting tolerances and other practical limitations. On the other hand, doing so is also not desirable. This is because when two electrodes are brought very close to each other, the surface roughness of the electrodes and the tilt in the electrodes will negatively affect the performance of the sensor itself. Due to the above mentioned reasons, the

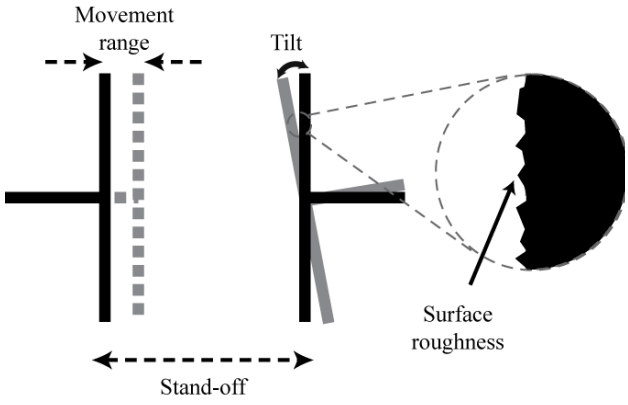

Fig. 1. Parallel plate capacitive sensor and the associated non-idealities.

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minimum electrode distance is expected to be in the order of 10 um for such applications. This means that the capacitance variation is roughly 3 orders of magnitude smaller than the nominal sensor capacitance. In other words, if the ratio of the capacitance variation to the nominal sensor capacitance is of interest, the measurement range is quite small.

The resolution requirement for the readout electronics is adversely affected. If 10 pm position resolution is required, the capacitive ratio needs to be measured with 20 bit resolution. It is thus desirable that the fact that the measurement range is limited can be utilized to relax the specifications of the readout electronics, so that an effective resolution of 20 bit can be achieved without several sacrifice in measurement time or power consumption.

III. THEORETICAL BACKGROUND

The proposed capacitive ratio measurement method does not rely on balancing the charge from two capacitances over time, as the traditional sigma-delta technique does. Instead, the ratio measurement is achieved by two separate measurements that share a portion of the same amplification factor. This is illustrated by fig. 2.

C_1 corresponds to the sensor capacitance, while C_2 is a capacitance equals to the nominal value of C_1. This is because C_2 is used to cancel the offset capacitance of the sensor, as shown in fig. 2 (a): The effect of the offset capacitance are cancelled electrically by connecting a fixed capacitance to form a capacitance half bridge and drive the two ends of the half bridge with anti-phase excitation signal. To the common end of the capacitive half bridge, the equivalent capacitance is to a very good approximation equal to C_1-C_2 if a good virtual ground node is provided.

The first measurement yields a result that is proportional to C_2/C_f ; a subsequent measurement gives result that is proportional to $(C_1\text{-}C_2)/C_f$. By keeping in mind the difference in the gains of the two measurements, the ratio $(C_1\text{-}C_2)/C_2$ can be obtained, which is related to the desired ratio C_1/C_2 as indicated in (1).

$$\frac{C_1}{C_2} = 1 + \frac{C_1 - C_2}{C_2} \tag{1}$$

To find out how the resolution of C_1/C_2 is related to the two separate measurements, the error propagation theory needs to be applied. For convenience, denote:

$$\begin{aligned} \alpha &= \frac{C_1 - C_2}{C_2} \\ \beta &= \frac{C_1}{C_2} \\ \theta &= C_1 - C_2 \\ \varphi &= C_2 \end{aligned} \tag{2}$$

so that:

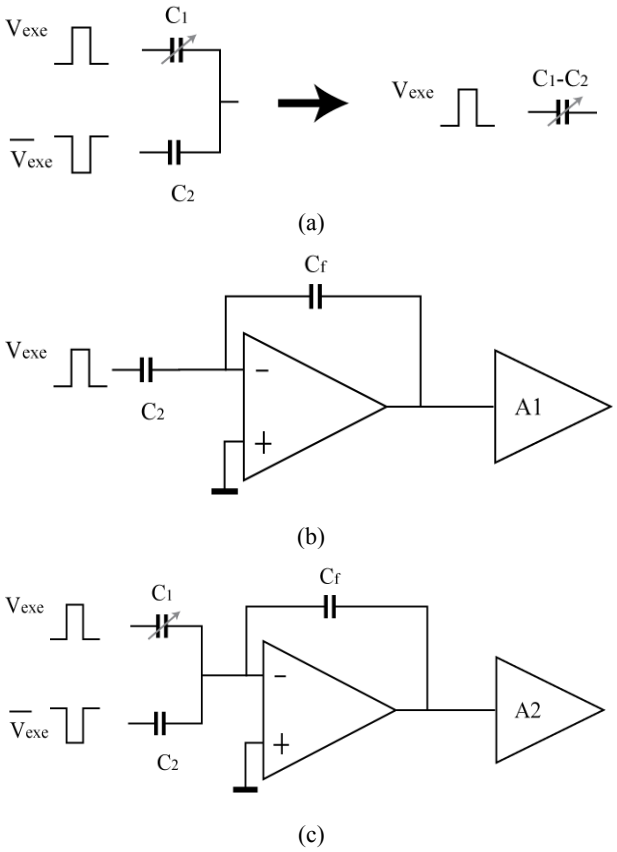

Fig. 2. (a) cancelling the offset capacitance; (b) measuring C_2 along; (c) measuring C_1-C_2.

$$\begin{aligned} \alpha &= \frac{\theta}{\varphi} \\ \beta &= 1 + \alpha \end{aligned} \tag{3}$$

Using error propagation formula [3]:

$$\sigma^2(\beta) = \sigma^2(\alpha) \tag{4}$$

and:

$$\sigma^2(\alpha) = \left(\frac{1}{\varphi}\right)^2 \cdot \sigma^2(\theta) + \left(\frac{\theta}{\varphi^2}\right)^2 \cdot \sigma^2(\varphi) \tag{5}$$

It can be seen from (5) that the variance in θ measurement is desensitized by a factor equal to φ^2, and hence has relaxed requirement; furthermore, if θ is much smaller than φ, the measurement noise in φ will hardly affect the variance in the ratio measurement.

As a numerical example, suppose φ (C_2) has nominal value of 10 pF; while θ (C_1-C_2) is smaller than 100 fF. If the measurement resolution in θ is 10 aF, it corresponds to a SNR requirement of 80 dB, or 13 bit. If at the same time the measurement resolution in φ is kept below 100 aF, which corresponds to a SNR requirement of 100 dB, the overall resolution in β measurement can achieve

approximately 1 ppm, corresponding to 20 bit. The dominant source of error then comes from θ measurement in this example.

The significance in this is that high effective resolution can be achieved with two relatively low resolution measurements. Thus the severe tradeoff between resolution and power consumption or measurement time is avoided. The required measurement resolution is within the reach of fast, Nyquist-rate conversion principles, such as SAR.

It can be also seen from (5) that the performance of the proposed measurement method depends heavily on the matching between C_1 and C_2. Even when the variation range of C_1 is small, if there exists a big mismatch between C_1 and C_2 so that θ is big, the measurement error in φ cannot be effectively suppressed. In other words, the best resolution is achieved close to the capacitance region where $C_1 \approx C_2$. In practice, this means that C_2 should be adjustable to accommodate the tolerance of the nominal sensor capacitance. In most cases, this drawback is acceptable.

Other measurement errors, such as offset and gain error will also introduce error in the derived ratio. Depending on the applications, the tolerance for such errors may be different. This should be taken into consideration as well.

In order to verify the validity of the above analysis, as well as to include more error sources, a numerical model is built in Matlab. In the following section, the model will be introduced in detail, and the simulation results will be shown and analyzed.

IV. Simulation Results

A. Error Model.

The purpose of the model is to quickly give answers about the effects of different errors on the quantity of interest. Therefore a macro model is enough, and would serve as a tool to help extracting the specifications of circuit level design that follows.

To clearly see the effects of different kinds of errors, it makes sense to first classify the error sources and observe their effects separately. The total effects are checked later.

From the previous section, it can be seen that the most effective way to conduct the measurement is to measure C_1-C_2 and C_2 separately, from which the desired ratio $\alpha = (C_1\text{-}C_2)/C_2$ is obtained. In this way, the requirements for both measurements are relaxed, yet the effective resolution is still very high. The macro model follows exactly the same procedure, and different types of errors are introduced in different steps.

In reality, the huge difference in the range of C_1-C_2 and C_2 demand for additional gain stage after the front-end to be added to be able to adjust the total gain. The gain of the additional gain stages will generally be determined by on-chip capacitance ratios, and hence can be quite stable and accurate. However, gain error in the order of hundreds of ppm should be expected. It is thus important to see how the gain error would affect the final result to get a quantitative specification on the tolerable gain error and gain error drift. If it turns out that such gain error is not tolerable, trimming the gain becomes mandatory.

Fig. 3 shows the diagram of the implemented error model and how different errors are added. The included

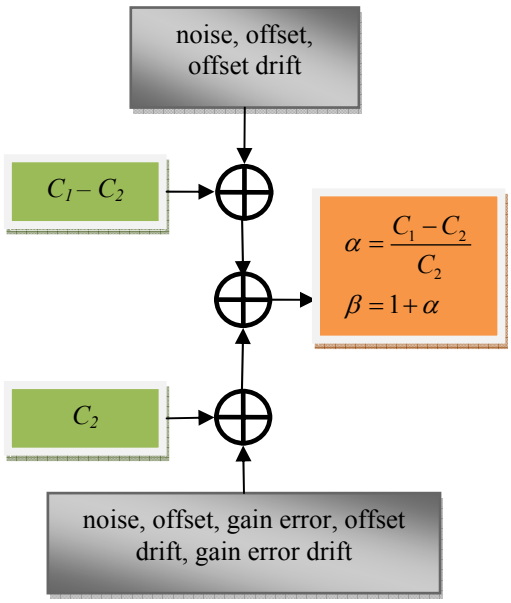

Fig. 3. Schematic of the error model

errors can be classified into two groups: random error and deterministic error. The former includes measurement noise, which determines the measurement resolution, while all other errors are considered deterministic error. Deterministic errors do not directly affect resolution, but can affect measurement precision. At first only random error is considered to see verify the resolution of the proposed measurement. The effect of deterministic errors is studied later in the context of a specific application.

Fig. 4 shows the simulated standard deviation of ratio β

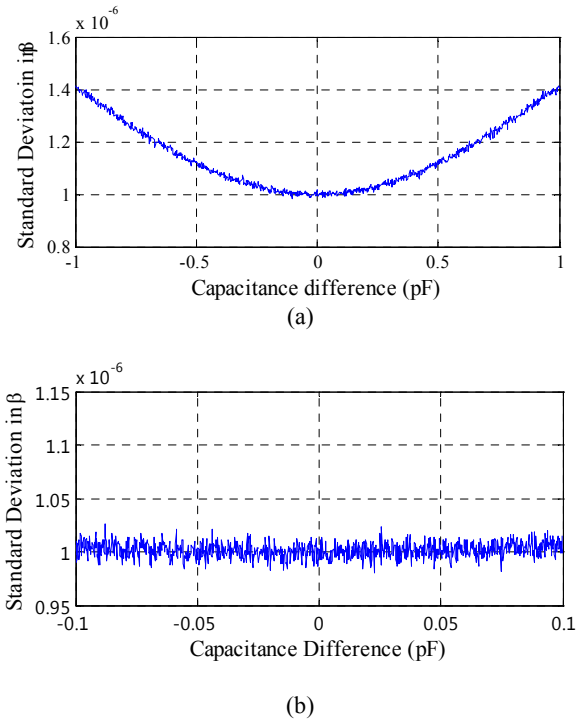

Fig. 4. Simulated standard deviation in the obtained capacitive ratio as a function of the difference between C_1 and C_2.

as a function of C_1-C_2. The simulation conditions are 10 aF standard deviation in C_1-C_2 measurement and 100 aF standard deviation in C_1-C_2 measurement. As can be seen, when the difference between C_1 and C_2 is below 0.1 pF, the standard deviation in β is essentially constant and around 10^{-6}. Given that the nominal value of β is 1, this corresponds to 1 ppm resolution, or 20 bit. The theory is thus verified. From fig. 4 (a), it can be seen that even with capacitance mismatch of 1 pF, the maximum standard deviation is increased by a factor of square root of 2. Actually, at C_1-C_2 = 1 pF, the contribution from measurement noise of the two measurements are equal. This explains the coefficient of square root of 2.

The effects of the deterministic errors are studied when the derived capacitive ratio is used to interpret the change in the distance between the capacitive sensor electrodes. The stand-off distance is assumed to be 10 µm. The measurement range is ± 10 nm. The nominal value of C_1 is assumed to be 10 pF. And the maximum mismatch between C_1 and C_2 is assumed to be 0.1 pF, which is practical to achieve. The model provides links between different types of errors and the error in the final result. Table 1 listed the tolerable errors for a maximum error of 2.5 pm in the final interpreted distance variation, which is in line with the resolution requirement. It can be seen that the requirements on the listed deterministic errors are not extremely stringent. This again verifies the validity of the proposed measurement method.

TABLE 1. ERROR BUDGET

C_X-C_Z	Offset	<0.1 %
	Offset drift	<10 ppm
C_Z	Offset	<200 ppm
	Offset drift	<20 ppm
	Gain error	<200 ppm
	Gain error drift	<20 ppm

Take both random error and deterministic error into account, the total error is simulated and given in fig. 5. It can be seen the measurement accuracy is within ±80 pm.

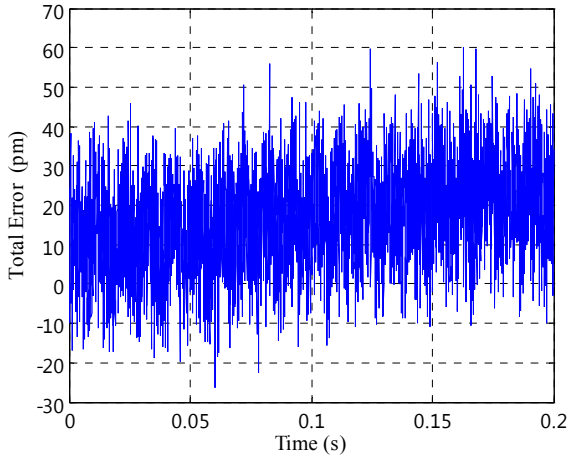

Fig. 5. Simulated total measurement error in distance variation

The error is dominated by (peak-to-peak) random error in the measurement.

V. CONCLUSION

A new approach to high resolution capacitive ratio measurement is presented. This method is well suited for applications where capacitance variation is much smaller than the nominal capacitance. The theory behind is explained and simulation results verify the concept. The authors are at the moment busy with implementing the system.

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